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MOU BETWEEN PHILIPS SEMICONDUCTORS, NETHERLANDS and IIT DELHI FOR CREATION OF PHILIPS CHAIR PROFESSOR FOR MICROELECTRONICS AT IIT DELHI

This memorandum of understanding made at this day, the 5th of August 1996 between Philips Semiconductors, Netherlands, 5600 MD Eindhoven, The Netherlands, hereinafter referred to as "Philips" and the Indian Institute of Technology Delhi, having its office at Hauz Khas, New Delhi, hereinafter referred to as "IITD" witnesseth as follows:

1. Objective

The main objective for which the perpetual position of Professor will be created is to promote research and academic work in the area of "Microelectronics and VLSI Design Tools and Technology".

2. Title:

The perpetual position of Professor will be designated as Philips Professor and will be henceforth referred to as "Professor" in this Memorandum.

3. Grant for Philips Chair:

Philips shall make available an amount of Rs.20,00,000 (Rupees twenty lacs only) to the IITD as a one-time grant for the sole purpose of partially supporting the position of Professor at IIT Delhi to achieve the objective stated above.

4. Utilization of the Grant:

The amount will be utilized for the purpose of partially meeting the expenditure in relation to the objective stated above.

5. Mode of Selection and Appointment of Professor:

A committee consisting of the following will make appointment to the Chair:

a) Director.
b) One nominee of the Board of Governors of IITD.
c) One nominee of Philips.
d) One senior faculty from IITD interested in Microelectronics and VLSI Design Tools and Technology, to be nominated by the Director.
e) One senior faculty from the concerned Department of the Institute in which the Chair is to be located, to be nominated by the Director.

The Philips Professor is expected to fulfil the normal obligations of a Professor in the Department, with research and development efforts oriented towards the objective of the Chair.

The IITD shall take steps to ensure that the Professor of Philips Chair is appointed as early as possible and agrees to initiate action to locate a suitable inclumbent within 15 days of the receipt of grant as per procedure outlined in Paara (5) above.

6. Tenure:

The tenure of the Professor will not exceed five years at the time of appointment and subsequent extensions, each for a further period of up to five years, will be subject to the review of the performance judged as satisfactory by Philips and IITD.

7. Presentation of the work done by the Professor:

Once in two years, the Professor should present his work in public, the place being chosen by Philips and IITD - it can be an International Conference.

8. Annual Report by the IITD:

After the end of each academic year, the Philips Professor placed at IIT Delhi will send a copy of the report and the work undertaken by him during the previous year.

IN WITNESS WHEREOF the parties hereto have signed this Memorandum of Understanding by the hand of Managing Director of Philips Semiconductors, on behalf of Philips and by the hand of Director IIT Delhi on behalf of IITD on the day, month and year referred to above.

SIGNED AND DELIVERED
on behalf of the said
PHILIPS SEMICONDUCTORS
NETHERLANDS

SIGNED AND DELIVERED
on behalf of the said
INDIAN INSTITUTE OF TECHNOLOGY
DELHI

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AGREEMENT

Between

Philips Semiconductors International B.V., having its registered office at Hurksestraat 9, 5652 AH, Eindhoven, the Netherlands (hereinafter referred to as "Philips Semiconductors")

and

Indian Institute of Technology Delhi, having its registered office at Hauz Khas, New Delhi 110016 (hereinafter referred to as "IIT Delhi").

(Philips Semiconductors and IIT Delhi hereinafter individually referred to as "Party" and collectively as "Parties").

WHEREAS, Philips Semiconductors is in the worldwide business of the development, manufacture and sale of a broad range of semiconductors and is interested in establishing a design competence centre in India;

WHEREAS, IIT Delhi is a well reputed technological university institute, which is a.o. conducting and promoting research in the field of VLSI Design Tools and Technology).

WHEREAS, the Parties are interested in cooperating by means of setting up a design laboratory in India and furthermore by sponsorship of a certain number of student candidates for a proposed multi-industry program titled "VLSI Design, Tools and Technology";

THEREFORE, PARTIES HERETO NOW AGREE AS FOLLOWS:

ARTICLE 1
DESIGN LABORATORY

1.1 Philips Semiconductors will set up at the IIT Delhi site a design laboratory (hereinafter referred to as "Philips Semiconductors Design Laboratory") consisting of a network of workstations, VLSI design tools and DSP development tools. Philips Semiconductors will free of charge install in and consign to the Philips Semiconductors Design Laboratory the hardware, including a three years hardware maintenance contract, and install on the hardware certain Philips proprietary software (hereinafter referred to as "Software"). The Software shall remain the property of Philips Semiconductors and Philips Semiconductors grants a right to the Philips Semiconductors sponsored students and designated IIT Delhi staff to use the Software only within the Philips Semiconductors Design Laboratory and in the framework of the Program (as hereinafter defined). The access to the above referenced laboratory will be restricted with a view to protect the Software. This will be done by IIT Delhi installing appropriate hardware and software which will permit access only from certain designated terminals and by persons authorized to "log-in" from such terminals.

1.2 IIT Delhi will provide at its costs appropriate facilities for the Philips Semiconductors Design Laboratory and will furthermore at its costs be responsible for maintenance of such facilities in order to keep them fit for their purpose as design laboratory. Philips Semiconductors will pay to IIT Delhi a one-time Rs. 300,000 for refurnishing and preparing the facilities so as to make them fit for their purpose as a design laboratory.

1.3 The Philips Semiconductors Design Laboratory shall be accessible to the following categories of users:

a. Philips Semiconductors sponsored M.Tech students
b. faculty, academic staff members/students working on Philips Semiconductors sponsored projects
c. any Philips Semiconductors employee deputed to IIT Delhi for the program
d. faculty members associated with the M.Tech Program for work of academic nature (i.e. not sponsored by any industry)
e. non-sponsored under graduate and post graduate students working with the associated faculties on project of academic nature (i.e. not sponsored by any industry). IIT Delhi shall develop and establish a protection mechanism which shall allow only the class of users in a., b. and c. above to access the Software. These users shall be required to sign the Non-Disclosure Agreement in Annex 3.

ARTICLE 2

M.TECH PROGRAM

2.1 Philips Semiconductors will sponsor 10 candidates each of the first two years of the term of this Agreement for the IIT Delhi M.Tech program on VLSI Design Tools and Technology (hereinafter referred to as "the Program"). The sponsorship fee will amount to Rs 200,000 for each candidate admitted to the Program and sponsored by Philips Semiconductors. In addition to the sponsorship fee, Philips Semiconductors will pay a stipend of Rs. 4,000 per month and contingency grant of Rs 10,000 per year per candidate.

2.2 IIT Delhi will select candidates for the Program and provide student accommodation on the IIT Delhi campus.

2.3 The hostel room rent for each candidate selected for the Program will be paid from the sponsorship fee, while each such candidate will have to pay its own boarding expenses.

2.4 Each student registered for the Program will be governed by the rules and regulations applicable to all full-time students.

2.5 Further details on the Program are set out in Annex 1 attached hereto.

2.6 In case a Philips Semiconductors sponsored student leaves the Program, IIT Delhi bears no other responsibility than the obligation to restitute to Philips Semiconductors such part of the fees mentioned in Article 2.1 of this Agreement proportional to the remaining period of the Program in which such sponsored student will no more participate.

ARTICLE 3

INTELLECTUAL PROPERTY RIGHTS

3.1 For the purpose of this Article 3 the following definitions will apply:

"Information" means drawings, specifications, photographs, samples, models,

processes, procedures, instructions, reports, papers, correspondence and any other technical or commercial information, data and documents of any kind, and including oral information if confirmed in writing within 30 days after the disclosure thereof, but excluding any Intellectual Property Rights pertaining thereto.

"Intellectual Property Rights" means patents, petty patents, utility models, design patents (both registered and unregistered), design rights, copyrights, know-how and any other form of intellectual property right protection afforded by law to inventions, designs or technical information, and applications therefor.

"Background Information" means such Information (other than Foreground Information), whether scientific or technical, which at the date hereof is or during the continuance of the Program comes into the ownership or control of a Party or of any of its affiliated companies and which such Party is free to disclose without the consent of or need to account to any third party.

"Background Intellectual Property Rights" means Intellectual Property Rights (not being Foreground Intellectual Property Rights) which at the date hereof are or during the continuance of the Program come into the ownership or control of a Party or any of its affiliated companies and under which such Party is free to grant licenses without the consent of or need to account to any third Party.

"Background" means Background Information and Background Intellectual Property Rights.

"Foreground Information" means such information, whether scientific or technical, as is generated by a Party and/or one or more Philips Semiconductors sponsored students in the framework of the Program.

"Foreground Intellectual Property Rights" means such Intellectual Property Right as are generated by a Party and/or one or more Philips Semiconductors sponsored students in the framework of the Program.

"Foreground" means Foreground Information and Foreground Intellectual Property Rights.

3.2 Both Parties will provide such necessary Background to the Program that both Parties agree is required to enable the other Party to carry out the Program, such Background to be described in accordance with Annex 2. For the avoidance of doubt it is stated that all Background used in the execution of the Program shall remain the property of the Party providing the same.

3.3 Foreground created during the Program by one or more employees of Philips Semiconductors and/or by one or more students sponsored by Philips Semiconductors and/or one or more IIT Delhi faculty members in the framework of the Program shall vest in Philips Semiconductors, and to the extent necessary, shall be transferred to Philips Semiconductors forthwith after the creation of such Foreground. In respect of inventions as part of the Foreground, Philips Semiconductors shall file the patent application in such countries it may choose, while explicitly mentioning in the patent application the name of the inventor(s) subject to section 39 of the Indian Patents Act, 1970.

3.4 IIT Delhi shall arrange that each and every student participating in the Program and furthermore those students making use of the Philips Semiconductors Design Laboratory shall sign the Non Disclosure Agreement as attached hereto in Annex 3.

ARTICLE 4

CONFIDENTIALITY

4.1 Any Information disclosed by Philips Semiconductors to IIT Delhi and/or to any Philips Semiconductors sponsored or other non-sponsored students participating in the Program, relating to the Program, is confidential and proprietary information ("Information") and is subject to the confidentiality provisions of this Agreement.

4.2 Subject to Article 6 (Publication) below, both Parties agree to keep Information in confidence and not to disclose it to third parties. Both Parties further agree not to use Information in any way other than performing its obligations pursuant to this Agreement.

4.3 Both Parties undertake to protect Information with at least the same degree of care used to protect its own proprietary Information against disclosure, replication, unauthorized use, copying or misappropriation and shall make the IIT Delhi Program Coordinator responsible for monitoring this compliance with such duties of protection of the Information.

4.4 IIT Delhi shall maintain all copies of the Software under the custody and control of the IIT Delhi Program Coordinator who shall maintain a written inventory uniquely identifying each copy. All Information, including said Software, shall be maintained in the Philips Semiconductors Design Laboratory in a secure locked place.

4.5 IIT Delhi shall designate to Philips Semiconductors those individuals belonging to the categories mentioned in Article 1.3 of this Agreement, who shall have execution access to the Software furnished by Philips Semiconductors. All such individuals designated for such access shall, prior to being allowed actual access, execute a confidentiality agreement containing similar confidentiality and protection against unauthorized use, copying, replication and misappropriation obligations as set forth in this Article 4.

4.6 Promptly at the termination or expiration of this Agreement, IIT Delhi shall submit all Information to Philips Semiconductors and/or where appropriate, shall destroy or erase Information such that IIT Delhi retains no copies thereof (in whatever form, including electronic) and no written materials relating to the specifications or content of the materials supplied by Philips Semiconductors to the Program.

4.7 The confidentiality provisions of this Agreement shall not apply to any Information which:

a. as shown by reasonably documented proof was received by the Parties in good faith from a third party not subject to a confidentiality obligation to either Party;

b. as shown by reasonably documented proof was in the other Party's possession prior to receipt thereof from the other Party;

c. now is or later has become publicly known through no breach of confidentiality obligation by other Parties.

ARTICLE 5

PUBLICATIONS

Notwithstanding the provisions of Clause 4 above, Philips Semiconductors recognizes that members of IIT Delhi staff and/or Philips Semiconductors sponsored students participating in the Program may wish to publish information derived from the Program in the academic press and/or divulge such Information at academic meetings or symposia. Any such publication or disclosure may only be made after the written consent of Philips Semiconductors has been obtained and such consent, if given, should be given within two weeks of the receipt of written request. Philips Semiconductors will have the right to require a delay of such publication or disclosure in order to protect Philips Semiconductors' commercial interest.

Philips Semiconductors agrees that any delay in publication will be kept to a minimum and that its consent shall not be unreasonably delayed and that Philips Semiconductors will clearly indicate the reasons for such delay. Such consented publications or disclosures will carry an acknowledgement of the financial support of Philips Semiconductors unless waived in writing by Philips Semiconductors.

ARTICLE 6

DURATION

6.1 This Agreement shall become into full force and effect on the date of signing hereof by duly authorized representatives of both Parties and shall thereafter remain in effect for a period of three (3) years.

6.2 If either Party materially fails to perform or violates any obligation pursuant to this Agreement, then, upon thirty (30) days written notice to the breaching Party specifying such default, the non-breaching Party may terminate or suspend this Agreement, without liability, unless the breach specified in a notice has been cured within the thirty (30) days period.

6.3 If either Party becomes insolvent or bankruptcy proceedings are instituted against it or on its behalf or if either Party makes an unauthorized assignment for the benefit of creditors, such event shall entitle the other Party to immediately terminate this Agreement, to cease performance hereunder and to avail itself of any and all legal or equitable remedies it may have against the other Party.

ARTICLE 7

FORCE MAJEURE

In the event that either Party is delayed or impeded in the performance of its obligations hereunder by any cause beyond its reasonable control it shall be entitled to such extension of time for such performance as may be fair and reasonable in all the circumstances.

ARTICLE 8

LIABILITY

8.1 Both Parties shall use all reasonable endeavours to ensure the accuracy of the work performed and any Information given but the Parties do not warrant, express or implied the accuracy thereof and will not be held responsible for any consequences arising out of any inaccuracies or omissions unless such inaccuracies or omissions are the result of negligence by one of the Parties.

8.2 IIT Delhi acknowledges and agrees that Philips Semiconductors Information is provided by Philips Semiconductors "as is", and that Philips Semiconductors disclaims all warranties of any kind either expressed or implied, including without limitation warranties of merchantability and fitness for a particular purpose. Similarly, Philips Semiconductors acknowledges and agrees that IIT Delhi's Information is provided by IIT Delhi "as is" and the same conditions apply as above to IIT Delhi's Information.

8.3 In no event shall Philips Semiconductors be liable to IIT Delhi or any other person for any damage whatsoever arising in connection with its performance under this Agreement and/or out of or as a result of the use of Philips Semiconductors Information including any and all costs, expenses, including without limitation, special, incidental or consequential damages even if Philips Semiconductors has been advised of the possibility of such damages.

8.4 In no event shall IIT Delhi be liable to Philips Semiconductors or any other person for any damage whatsoever arising in connection with Philips Semiconductors' or any other third party's usage of work product developed and/or delivered as a result of the program created by this Agreement.

ARTICLE 9

WAIVER

The failure of a Party hereto to exercise or enforce any right conferred upon it under this Agreement shall not be a waiver of any such right nor operate to bar the exercise or enforcement thereof at any time thereafter.

ARTICLE 10

ENTIRE AGREEMENT

This Agreement including its Annexes sets forth the entire Agreement between the Parties as to the subject matter hereof and merges all discussion and negotiations between them. No modification or amendment of this Agreement including its Annexes shall be valid or binding unless made in writing and signed on behalf of the Parties by their duly authorized representatives.

ARTICLE 11

ASSIGNMENT

Neither this Agreement nor any right or obligation hereunder is assignable by one Party without the prior consent of the other which consent shall not be unreasonably withheld. It is however explicitly understood that Philips Electronics N.V., the ultimate parent company of the worldwide Philips Group of Companies is in the course of establishing a legal entity in the name of "Philips Software Centre Private Limited (PSC)", under Indian Law to which all the software related activities of the Philips Group in India will be transferred. Parties acknowledge that if, as and when such legal entity will have been established, Philips Semiconductors will assign all its rights and obligations under this Agreement to that new legal entity.

ARTICLE 12

ARBITRATION

In case of a dispute or difference between the Parties arising out of or in connection with the Agreement, the Parties shall first endeavour to settle it amicably by means of arbitration by two (2) arbitrators, one appointed by IIT Delhi and one appointed by Philips Semiconductors. Failing such settlement, any dispute shall be referred to the Indian Courts under Indian Law, explicitly excluding however any dispute concerning Intellectual Property Rights which shall be finally settled subject to the laws of the Netherlands under the rules of the Dutch Arbitration Institute, such arbitration to be held in Amsterdam, the Netherlands in the English language.

PHILIPS SEMICONDUCTORS B.V.

By

Name: Drs. R. P. KRAMER

Title: MANAGING DIRECTOR

Date: 5/Aug/96

IIT Delhi

By

Name: V.S. RAJU
Director
Indian Institute of Technology
Hauz Khas, New Delhi-110 016

Title:

Date:

ANNEX 1

Sponsored M.Tech program on VLSI Design, Tools and Technology

The following conditions shall apply to the Program

1. All Philips Semiconductors sponsored M.Tech students will do their major projects/thesis using the Philips Semiconductors Design Laboratory under the supervision of a faculty member associated with the Program. If required a co-supervisor from Philips Semiconductors would be co-opted for the Project. The projects would be assigned by mutual consent between Philips Semiconductors and the relevant IIT Delhi faculties associated with the Program. The completion of the project will be determined in accordance with the academic standards set by IIT Delhi.

2. IIT Delhi in collaboration with Philips Semiconductors instructors would arrange training for the Philips Semiconductors sponsored M.Tech students on the Philips Semiconductors design flow and the associated tools. This would be in the form of seminars/workshops and would be held during the first two semesters of that Program. The nature, duration, periodicity and appropriate course faculty for these training sessions will have to be mutually agreed upon by IIT Delhi and Philips Semiconductors.

3. The Philips Semiconductors representatives are eligible for membership of the M.Tech program Advisory Committee on a rotation basis among all sponsoring industries.

4. Further details on the contents of the Program are attached hereto in the "Proposal for an Industry Sponsored Interdisciplinary M.Tech Program in VLSI Design, Tools and Technology.

Proposal for an Industry Sponsored Interdisciplinary M.Tech. Programme in "VLSI Design, Tools & Technology"

Participating Departments/Centres :

Electrical Engg., Computer Science & Engg., Centre for Applied Research in Electronics and CEERI, Pilani (for technology training).

Programme Details :

As per the Institute norms the minimum credit requirements for the M.Tech. degree are 48 valid credits ('D' grades or above) including a minimum of 36 credits of course work and 12 credits of project work.

The programme is flexible to cater to the wide spectrum of background expected from the admitted students. The candidates can have a basic degree in Computer science (B.Tech. or equivalent) Electrical Engg. (B.Tech. or equivalent) Physics with electronics specialisation (M.Sc. or equivalent). The programme has three components namely background courses, core courses and elective courses. The background courses are expected to partially offset the deficiencies in inputs from different disciplines.

The programme would cater to the industry needs while taking care of the needs and requirements of each candidate. Some features of the programme are :

- A committee drawn out from the participating faculty would chalk out a program for each candidate.
- A non-credit practical training carried during the winter break. For candidates sponsored by industries interested in technology aspects, CEERI would expose the students to the device fabrication process.
- The major project in most cases is expected to be carried out at the sponsoring institute. The project typically would be supervised jointly by a faculty member and a senior person from the sponsoring industry.
- In specific cases background courses may be credited outside the list of courses enclosed, with the approval of the Program Coordinator.

List of background courses

1. MA 701 Introduction to Programming and Data Structures : 3 Credits (3-0-0)

Definition of the programme, Programming methodology, Concepts of structured programming. Definition and operations on arrays, stacks, queues, lists, trees. Evaluation of arithmetic expressions using stacks. List representation. Recursive and non-recursive definitions of tree structures. Operations using recursive and non- recursive algorithms. Forests. Simple searching and sorting algorithms. Hashing techniques.

2. MA 712 Numerical Analysis of Differential Equations: 3 Credits (3-0-0)

Solution of initial-value problems of systems of ODEs. Single step and multistep methods, convergence and stability analysis, choice of an algorithm and its computer implementation. Finite difference methods for the solution of two-point boundary-value problems and eigenvalue problems. Elliptic, parabolic and hyperbolic partial differential equations, convergence and stability analysis. Computer implementation.

3. PH 715 Physics of Semiconductor Devices : Credits 3 (3-0-0)

Semiconductor physics processes, rectifiers, varactors, switching diodes, Zener diodes, transistor, light emiting diodes, semiconductors, lasers, thermoelectric generators, Gun, superlattice, IMPATT and injection diode, MOS, FET and Schottky devices.

4. EE 733 Digital ICs and Systems: 3 Credits (3-0-0)

Noise considerations in Logic families, Digital system implementation using algorithmic state m/c concepts. Register transfer, busing, clocking and control, asynchronous and synchronous systems.

ALU. Control, semiconductor for memories and PLAs; microprogrammed and PLA based control unit design. Data transfer techniques, examples of I/O interface chips. Channel communication; protocols and standards, Methods in computer arithmetic.

5. EE 731 Digital Signal Processing I : 3 Credits (3-0-0)

Discrete time signals and systems. -transforms. Structures for digital filters. Design procedures for FIR and IIR filters. Frequency transformations: Linear phase design. Introduction to DFT. Errors in digital filtering. Hardware implementation cosiderations.

Core Courses

1. EE 732 Microelectronics: 3 Credits (3-0-0)

Brief recapitulation: Band theory, F-D statistics. Recombination effects and bipolar junction devices. MOS Devices; MOS capacitance - ideal characteristics. Interface effects and characterisation. MOSFET principles and characteristics. Various MOSFET structures, viz. MOS, VMOS etc. and some typical applications. Parasitic device effects in mosfet AND bipolar circuits.

Core Laboratory

Laboratory I : CS 745 High-level Digital Systems Design Lab : 3 credits (0-0-6)

Exposure to high-level design tools including high-level synthesis, logic synthesis and simulation. Modelling and design using VHDL. FPGA based design.

Laboratory II : EE 736 VLSI Physical Design Lab : 3 credits (0-0-6)

Introduction to CAD Tools. Circuit simulation using SPICE. Layout Design. Design Rules and Design Rule Checking. Design of a static CMOS inverter. Effects of W/L ratio on performance. Pseudo-NMOS inverters. Latchup and Layout considerations for its prevention. Transmission Gates. Circuit Characterization. Resistance and Capacitance Estimation. Gate Design. Static two-input NAND and NOR gates. Gate Transistor Sizing. Effects of and Fan-Out. Power dissipation and its Estimation using SPICE. Layout of complex gates. Dynamic, C2MOS, Pass-Transistor Logic. Domino, NP-Domino styles. Design Margining; effects of variations in supply voltage and temperature. Design Corners. Sizing of Power and Clock Conductors. Clocking Strategies.

One end-semester design project is also envisaged.

4. CS 746 Algorithm Analysis and Design: 3 credits (3-0-0)

Analysis of algorithms: What to analyse, order arithmetic, software timing and monitoring tools. Basic design methodologies; divide and conquer, dynamic programming, backtracking, greedy algorithms, Particular algorithms; set manipulation, matrix multiplication, pattern matching, integer and polynomial arithmetic. Fast Fourier transform, geometric algorithms, graph algorithms; NP completeness and theory of lower bounds; approximation algorithms.

5. CS 718 Architecture of Large Systems: 3 credits (3-0-0)

Classification of parallel computing structures. High performance memory system. Principles of pipelined computer systems. SIMD multiprocessor structures.

6. CS 712 Resource Management in Computer Systems: 3 credits (3-0-0)

Historical perspectives, interrupt mechanism, concurrent processes; mutual exclusion and synchronization. Process management, switching, scheduling and synchroniing. Memory management, swapping, segmentation paging, virtual memory, page replacement and space allocation policies, segmented paging, dynamic linking. File management, directory structure, basic file structures, system calls, secondary storage space management, terminal I/O handling, deadlocks, Protection, case studies.

OR

EE 753 Operating Systems: 3 credits (3-0-0)

Requirements and constraints of systems software. Influence of hardware platforms on systems programmers. Assembly language programming. Assemblers. One-pass and two-pass assembly. Symbol tables and macro handlers. Linkers and loaders. Object files, executable files, and libraries. Problems of memory management. Overlays. Introduction to language translators. Lexical analysis parsing, and code generation. Process management - Concurrent processes, mutual exclusion, synchronization, and scheduling. Memory management - concept of locality of reference, virtual memory, cache management, memory allocation algorithms. Resource management - Deadlock and its prevention. Fairness and priority. Protection. File management and I/O management. Elements of distributed operating systems.

7. CS 812 High-level Design & Modelling of Digital Systems : 3 credits (3-0-0)

System level design, architectural synthesis for DSP applications, behavioral modelling using VHDL, hardware-software partitioning, interface synthesis.

8. CS 814 FPGA based design : 3 credits (2-0-2)

Introduction to FPGA architectures, FPGA design flow, technology mapping for FPGAs, case studies.

Laboratory : Simple designs using FPGAs, exposure to tools for schematic capture, state ma-

and Scaling of Inter Connects. Statistical Modelling of Device and Circuits. Analog Computer Aided Design. Analog and Mixed Analog and Digital Circuits Layout.

14. EE 839 Memory Design and Testing: 3 credits (3-0-0)

Review of MOS Structure, Scaled Down MOSFET and CMOS Processing. Processing for Memories: Multipoly Floating Gate and Control Gate, Trench Capacitors and thin oxide. Inverter Design: Choice of W/L and Noise Margin Calculation, Cascode and Differential Inverters. SRAM and DRAM Cell Design: Basic Cell Structures, modelling and Design Equations. Sense Amplifiers: Necessity for Sense Amplifier, Voltage and Current Sense Amplifers, Reference Voltage Generation, Influence of Sense Amplifier Performance on cell architecture. Peripheral Circuits. Memory Testing: Modelling, Introduction to Functional Testing and Built in Self Test.

15. CR 702 Advanced IC Technology : 3 credits (3-0-0)

Introduction to crystal growth, epitaxial growth, Silicon Oxidation, thermal and rapid thermal oxidation, polysilicon oxidation and oxidation induced defects, Lithography: Optical-, E-beam-, X-ray-, Ion-beam- lithography Etching: Wet and Dry Etching, Reactive ION Etching, Ion Beam milling Physical and Chemical Vapour Deposition Thermal Diffusion, mechanisms, ION Implantation Process Integration: Isolation Techniques- Well Isolation, trench isolation, dielectric isolation LDD structures. PROCESS SIMULATION - SUPREM/STEPS/SAMPLE

16. CR 704 Advanced Process and Device Characterization (Measurements: 3 credits (3-0-0)

Physical Characterization: Thin Film Thickness- Measurements-ellipsometry, surface profiling, spectrophotometry, FTIR Critical Dimension Measurements: Optical microscope, Scanning Electron Microscope, Transmission Electron Microscope Material and Impurity Characterization: SIMS, XRD, EDAX Electrical Characterization: Four-probe technique, Hall effect, sheet resistance measurement. differential sheet resistivity, spreading resistance and impurity profiling C-V measurements, DLTS, Carrier lifetime, impurity profiling, I-V measurements and Process and SPICE model parameter Extraction

ANNEX 2

Background Description

Separate project agreements will be made wherein case by case the Background and transfer of such Background will be specified. Project owners from Philips Software Centre Private Limited will be assigned to each project.

ANNEX 3

Non Disclosure Agreement

Philips Semiconductors International B.V., having its registered office at Eindhoven, The Netherlands (hereinafter referred to as "Philips")

and

Indian Institute of Technology Delhi for the purpose hereof represented by ..... (hereinafter referred to as "IIT Delhi")

and

..... a student (hereinafter referred to as "the Student") participating in a multi-industry program titled VLSI Design, Tools and Technology at IIT Delhi (hereinafter jointly referred to as "the Program")

hereby agree that the following terms and conditions (hereinafter referred to as "Agreement") shall be applicable in connection with the activities in the framework of the Program, hereinafter called the "Authorized Purpose".

Clause I

Philips may disclose certain information to IIT Delhi and/or the Student with respect to the Authorized Purpose in writing, orally and/or otherwise. Such information may be, without limitation, in the form of business and/or financial records, presentations, specifications, samples, photographs, drawings or other documents. All information so disclosed is hereinafter referred to as "Confidential Information".

In case Confidential Information is disclosed in documentary or other tangible from, Philips will label same as "confidential", "proprietary", "copyright" or the like.

Clause II

All Confidential Information, which shall include any Derivatives therefrom, improvement thereon or translation, abridgement, adaptation or other change thereof by Philips and/or IIT Delhi and/or the Student, shall be the property of Philips.

Philips will provide all Confidential Information on an "as is" basis, without any warranty whatsoever, whether express, implied or otherwise, regarding its accuracy, completeness or otherwise, and Philips shall not be liable for any direct, special, incidental, consequential or other damages.

IIT Delhi and/or the Student will return all Confidential Information and any copies thereof to Philips immediately upon Philips' first written request.

Clause III

The parties agree that, unless Philips gives its prior written authorization, IIT Delhi and/or the Student shall, during a period of five (5) years from the date of disclosure of any Confidential Information hereunder:

a. not use the Confidential Information disclosed by Philips pursuant to Clause I for any other purpose than for the Authorized Purpose;

b. protect Philips' Confidential Information against disclosure in the same manner and with the same degree of care, but not less than a reasonable degree of care, with which it protects confidential information of its own;

c. limit circulation of the Confidential Information disclosed by Philips to IIT Delhi and/or the Student in connection with the Authorized Purpose.

In case of doubt IIT Delhi and/or the Student agree to request Philips in writing for latter's opinion.

IIT Delhi and/or the Student acknowledge that Philips will be irreparably harmed if IIT Delhi and/or the Student actually violate or threaten to violate their confidentiality obligations under this Agreement. Therefore, in the event of such actual or threatened violation Philips shall be entitled to an injunction or any other appropriate steps regarding any actual or threatened violation by the concerned persons of IIT Delhi and/or the Student.

Clause IV

The parties agree that information disclosed by Philips to IIT Delhi and/or the Student pursuant to this Agreement which would otherwise be Confidential Information shall not be deemed Confidential Information to the extent that it can be proven by written records that said information:

a. Is part of the public domain without violation of this Agreement;

b. is known and on record at IIT Delhi and/or the Student prior to disclosure by Philips;

c. is lawfully obtained by IIT Delhi and/or the Student from a third party who is not bound by similar confidentiality obligations;

d. is developed by IIT Delhi and/or the Student completely independently of any such disclosure by Philips;

e. is ascertainable from a commercially available product; or

f. is disclosed pursuant to administrative or judicial action, provided that IIT Delhi and/or the Student shall use their best efforts to maintain the confidentiality of the Confidential Information e.g. by asserting in such action any applicable privileges, and shall, immediately after gaining knowledge or receiving notice of such action, notify Philips thereof and give Philips the opportunity to seek any legal remedies so as to maintain such Confidential Information in confidence.

If only a portion of the Confidential Information falls under any of the above subsections, then only that portion of the Confidential Information shall be excluded from the use and disclosure restrictions of this Agreement.

Clause V

a. Nothing herein contained shall be construed as a grant by implication, estoppel or otherwise, of a license of any kind by Philips to the IIT Delhi and/or the Student e.g. to make, have made, use or sell any product using Confidential Information or as a license under any patent, patent application, utility model, copyright, maskwork right, or any other intellectual property right.

b. Intellectual property rights (meaning patents, petty patents, utility models, design patents (both registered and unregistered), design rights, copyrights, know-how and any other form of intellectual property right protection afforded by law to inventions, designs or technical information, and applications therefor) created by Student sponsored by Philips and/or IIT Delhi faculties members in the framework of the Program shall vest in Philips, and to the extent necessary, shall be transferred to Philips forthwith after the creation of such intellectual property right. In respect of inventions as part of the intellectual property rights, Philips shall file the patent application in such countries it may choose, while explicitly mentioning in the patent application the name of the inventor(s) subject to the provisions of Section 39 of the Indian Patents Act, 1970.

Clause VI

Written communications with respect to Confidential Information under this Agreement shall be addressed only to the following respective persons (or to such other person as either party may from time to time designate in writing):

Philips Semiconductors
International B.V.

F.a.o.:

Phone:

Fax:

IIT Delhi

F.a.o.:

Phone:

Fax:

Clause VII

IIT Delhi and/or the Student may not transfer or assign any or all of their rights and/or their obligations or delegate the performance of any or all of their obligations under this Agreement, directly or indirectly, through acquisition, merger or otherwise, without the prior written consent of Philips.